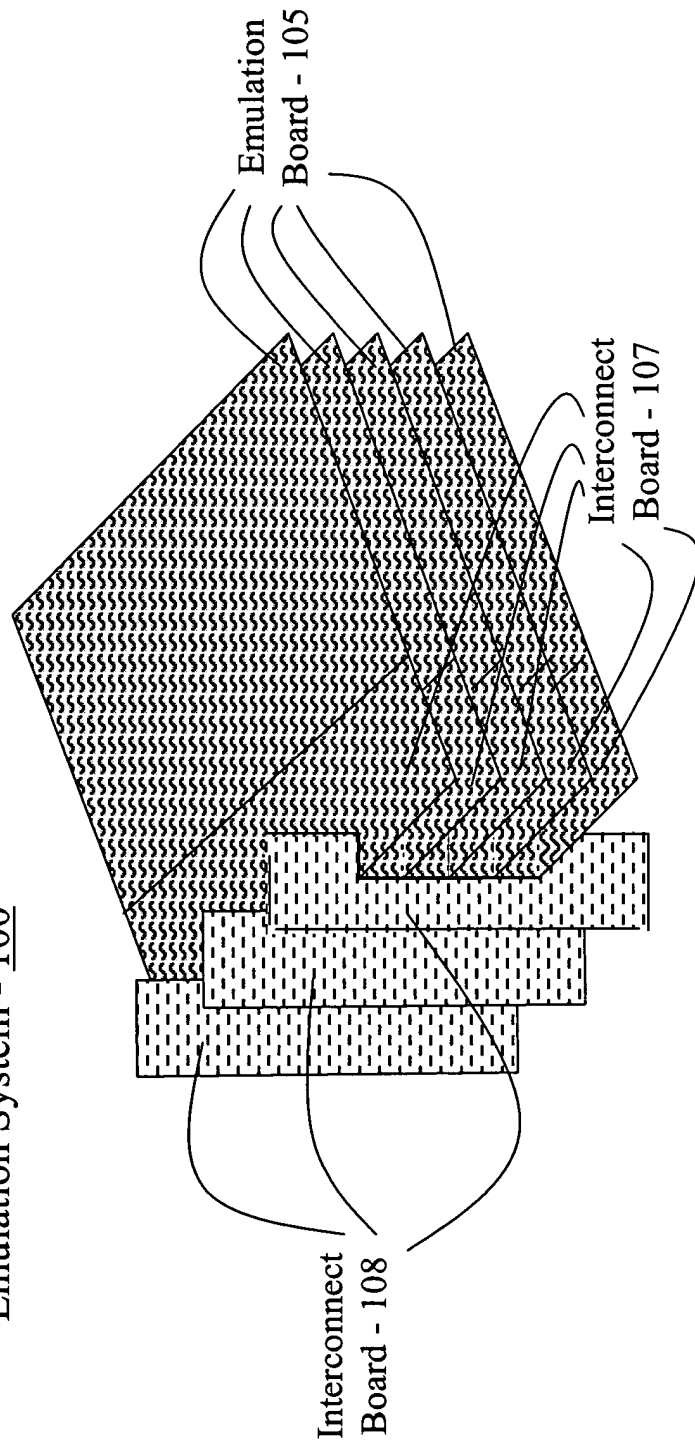


FIGURE 1

Emulation System - 100



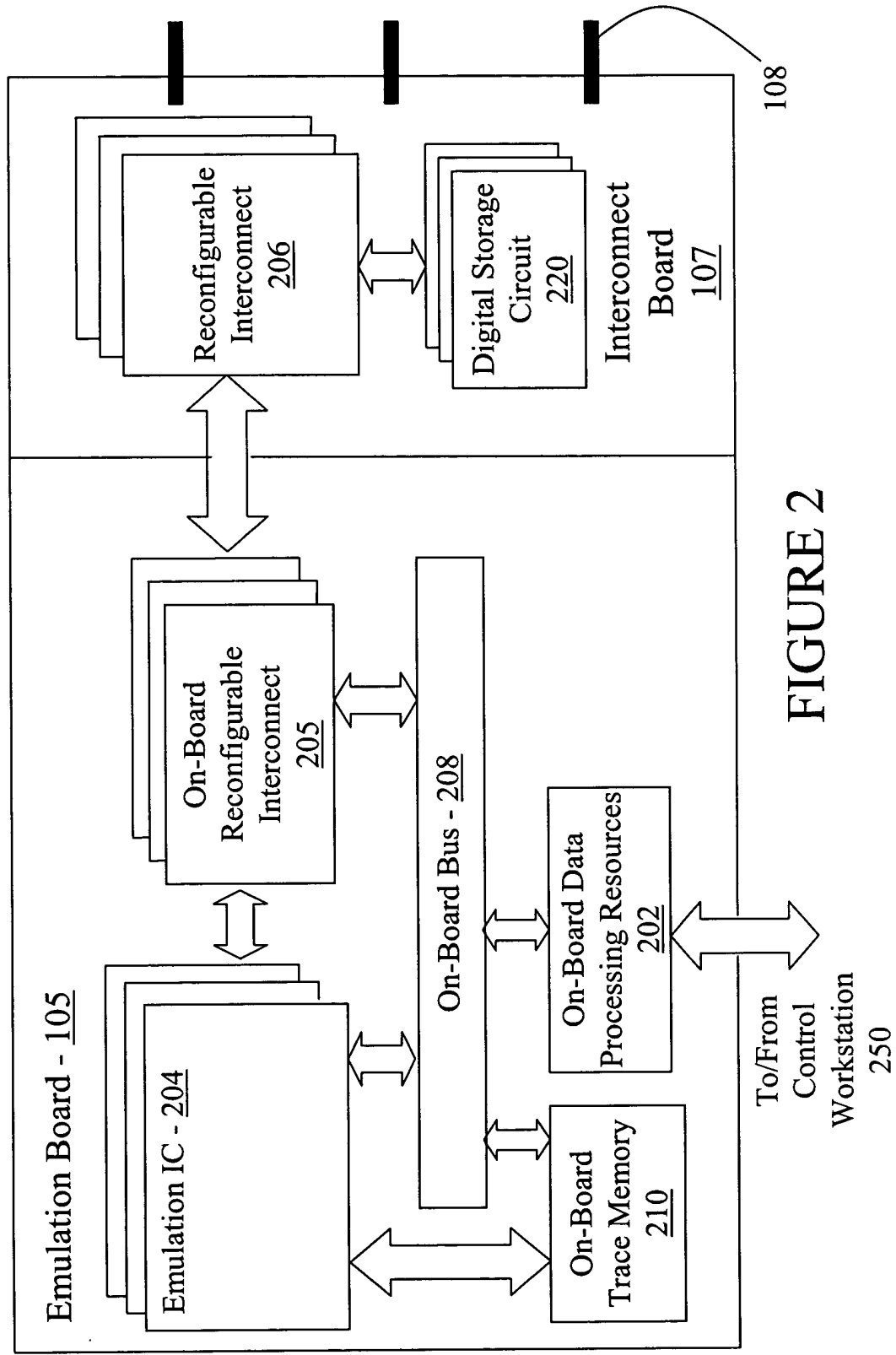


FIGURE 2

Figure 3

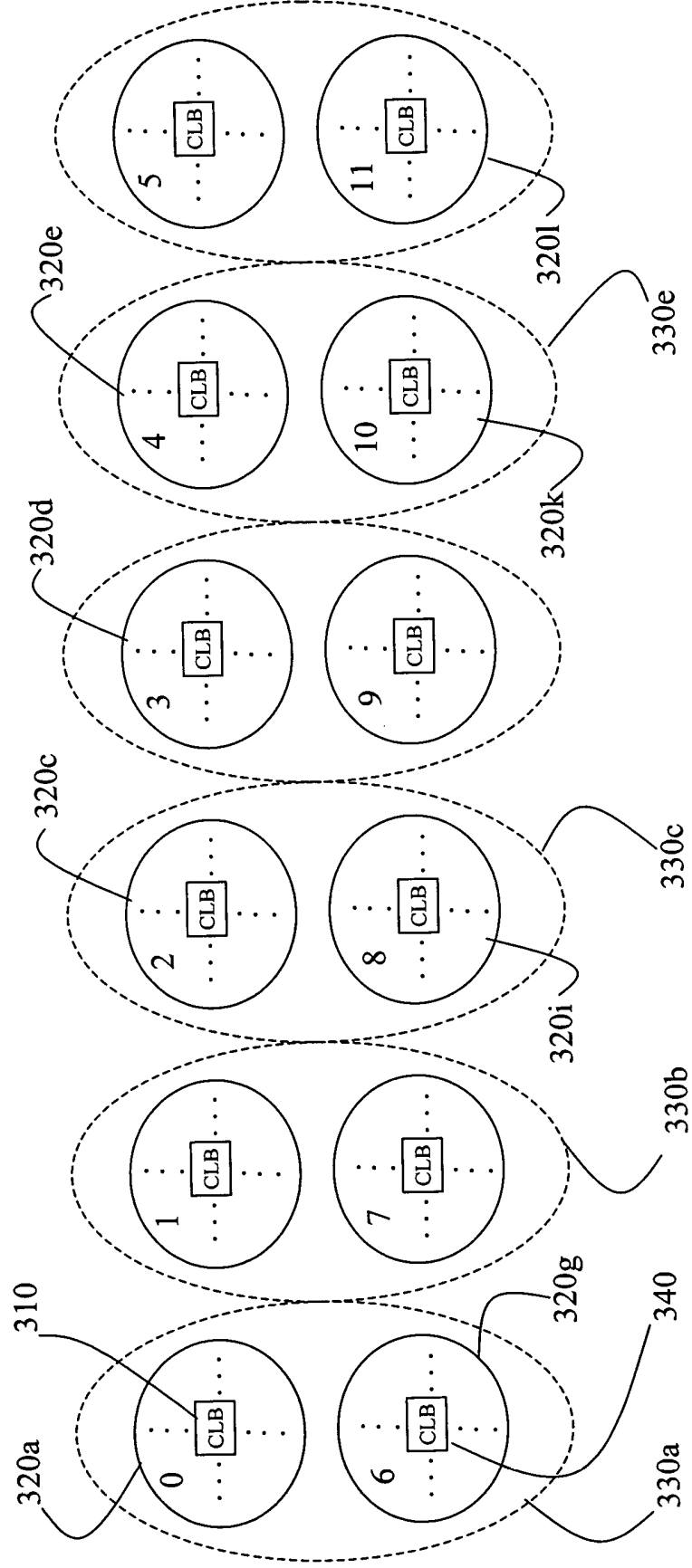
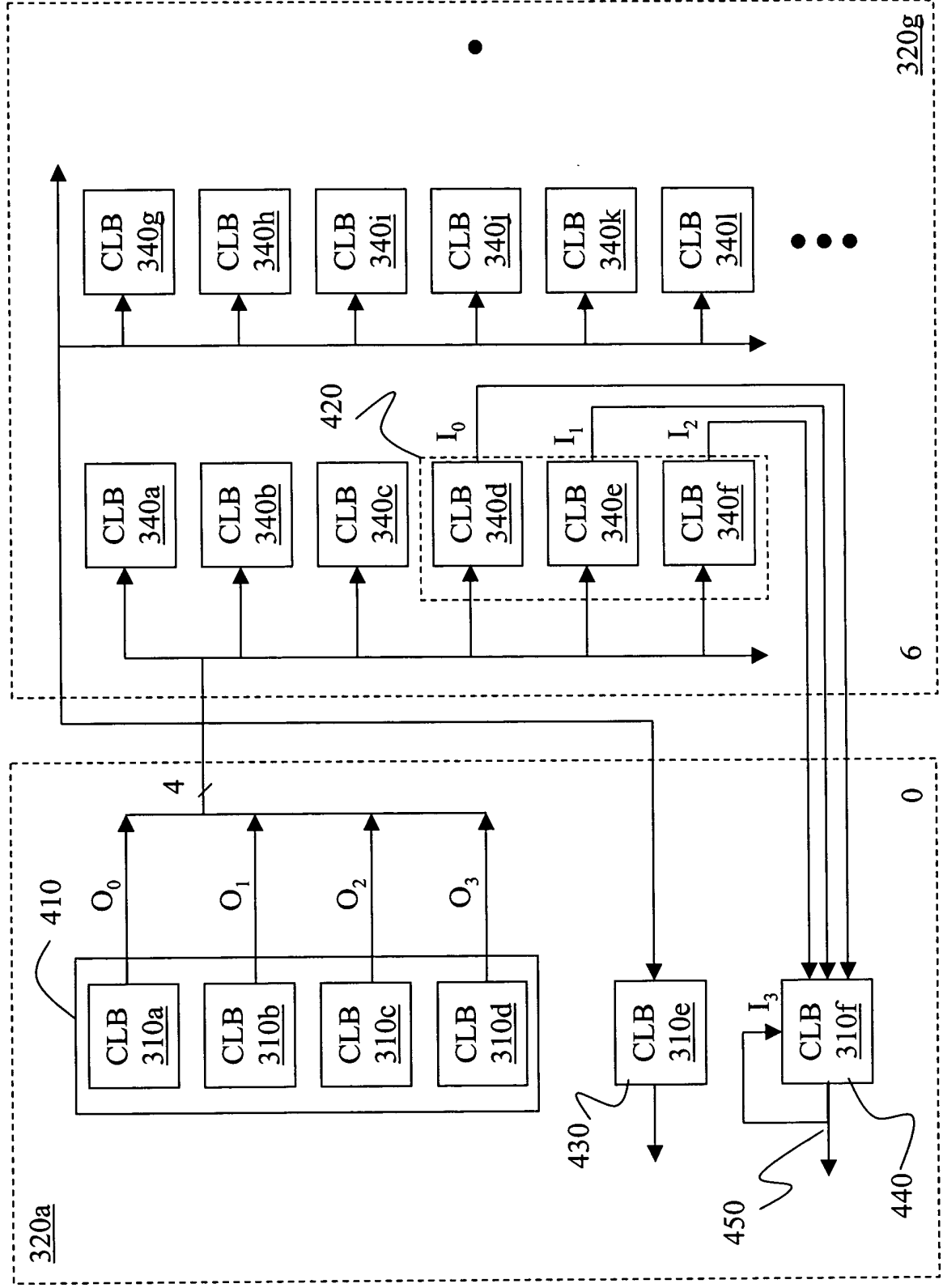


Figure 4



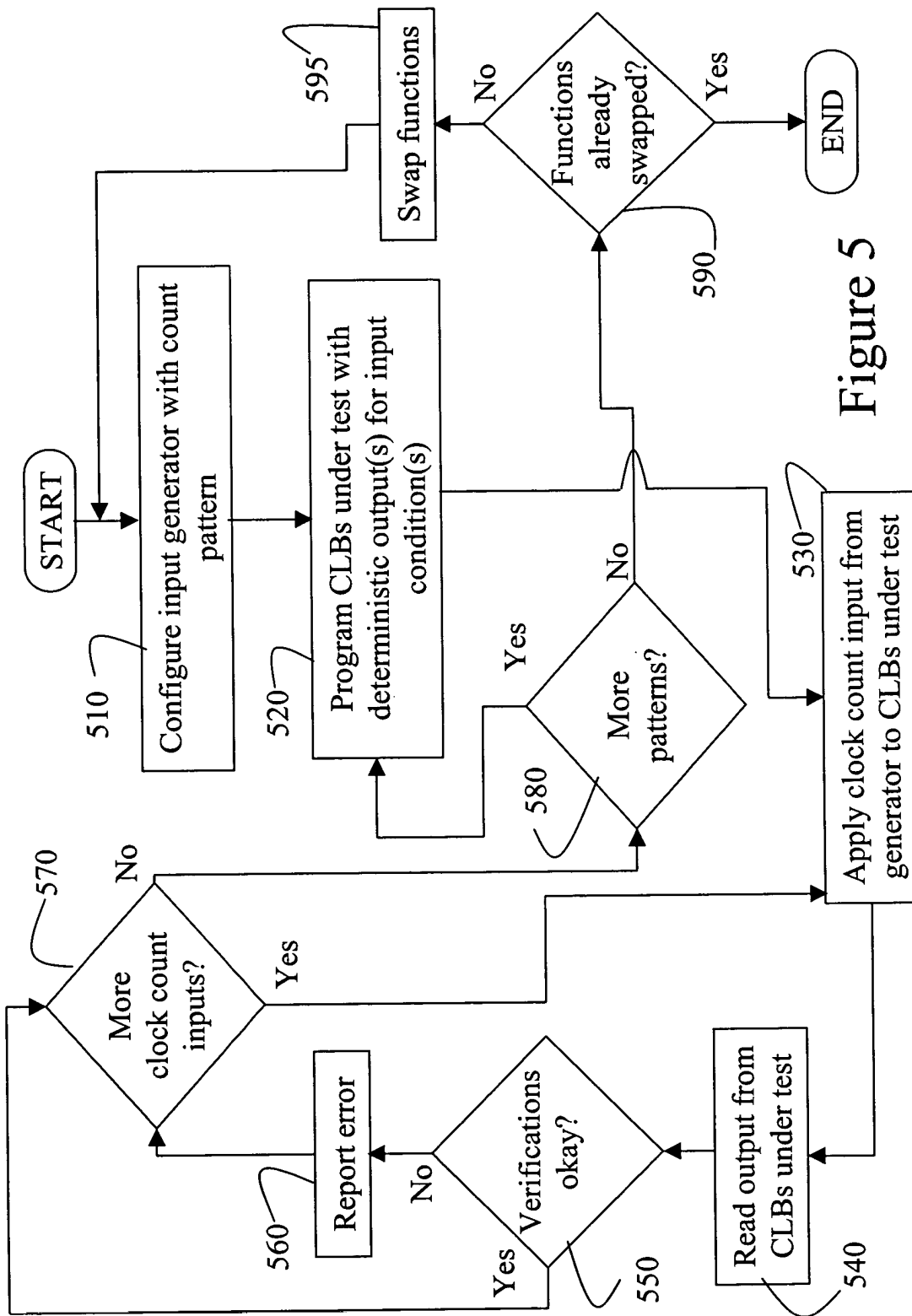


Figure 5

| Output of Input Generator 410 |                |                |                |   | CLB 340d | CLB 340e | CLB 340f |
|-------------------------------|----------------|----------------|----------------|---|----------|----------|----------|
| O <sub>3</sub>                | O <sub>2</sub> | O <sub>1</sub> | O <sub>0</sub> |   |          |          |          |
| 620                           | 0              | 0              | 0              | 0 | 1        | 1        | 1        |
| 630                           | 0              | 0              | 0              | 1 | 0        | 0        | 0        |
| 650                           | 0              | 0              | 1              | 0 | 1        | 1        | 1        |
|                               | 0              | 0              | 1              | 1 | 0        | 0        | 1        |
|                               | 0              | 1              | 0              | 0 | 1        | 1        | 1        |
|                               | 0              | 1              | 0              | 1 | 0        | 0        | 0        |
|                               | 0              | 1              | 1              | 0 | 1        | 1        | 1        |
|                               | 1              | 0              | 0              | 0 | 0        | 0        | 0        |
|                               | 1              | 0              | 0              | 1 | 1        | 1        | 1        |
|                               | 1              | 0              | 0              | 1 | 0        | 0        | 0        |
|                               | 1              | 0              | 1              | 0 | 1        | 1        | 1        |
|                               | 1              | 0              | 1              | 1 | 0        | 0        | 0        |
|                               | 1              | 1              | 0              | 0 | 1        | 1        | 1        |
|                               | 1              | 1              | 0              | 1 | 0        | 0        | 0        |
|                               | 1              | 1              | 1              | 0 | 1        | 1        | 1        |
|                               | 1              | 1              | 1              | 1 | 0        | 0        | 0        |

Figure 6

# Figure 7

| Tester Verification Pattern |       |       |       | Verifier |
|-----------------------------|-------|-------|-------|----------|
|                             | $I_2$ | $I_1$ | $I_0$ | 440      |
| 710                         | 0     | 0     | 0     | 0        |
| 720                         | 0     | 0     | 1     | 1        |
|                             | 0     | 1     | 0     | 1        |
|                             | 0     | 1     | 1     | 1        |
|                             | 1     | 0     | 0     | 1        |
|                             | 1     | 0     | 1     | 1        |
|                             | 1     | 1     | 0     | 1        |
|                             | 1     | 1     | 1     | 0        |

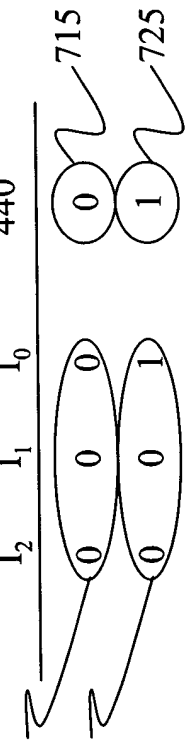
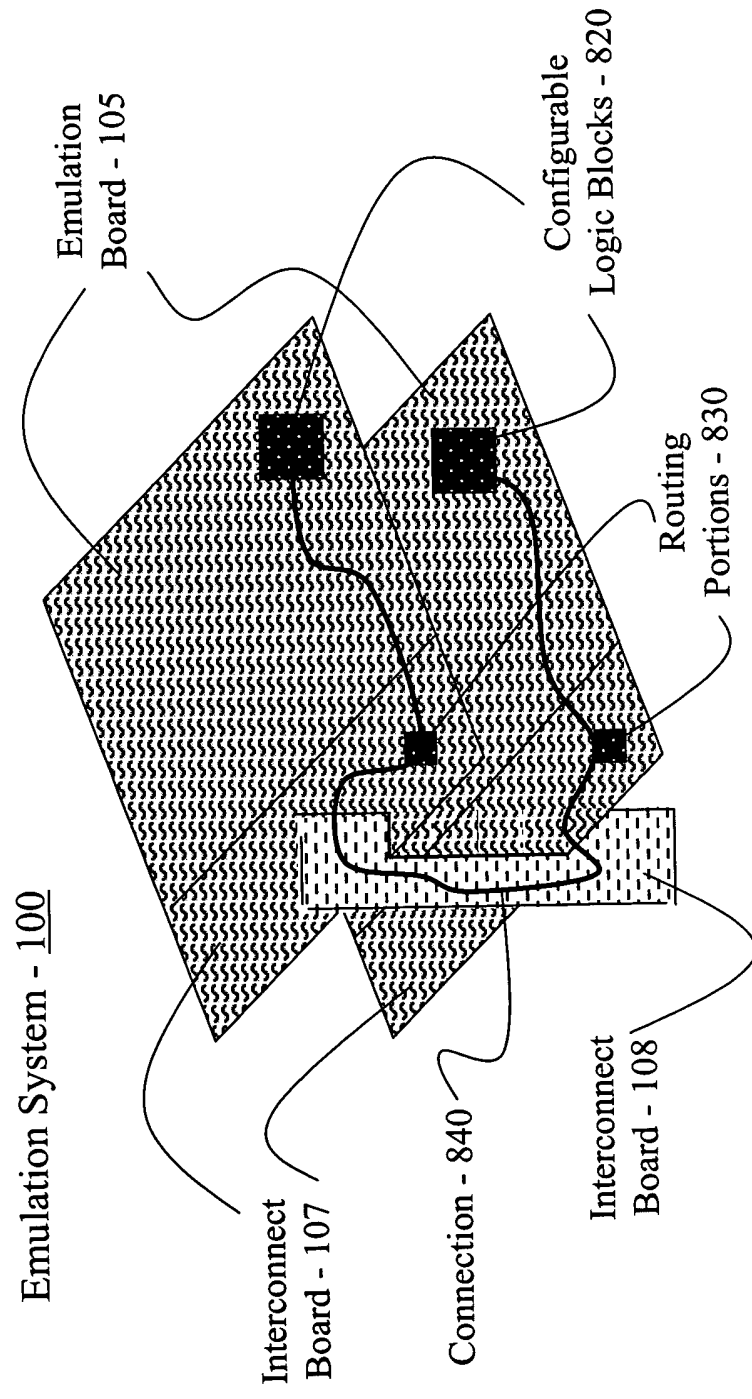


FIGURE 8A





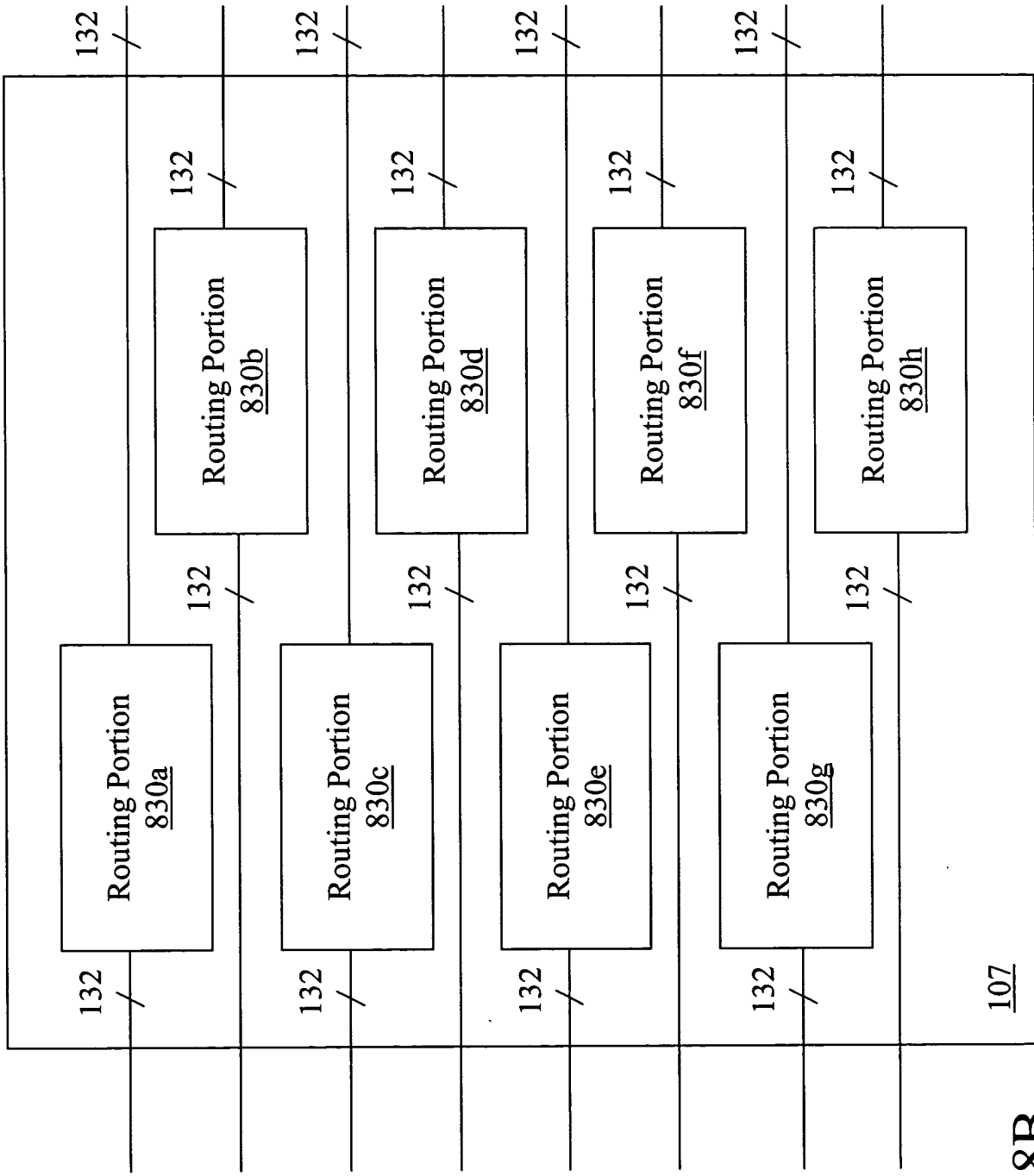


Figure 8B

Figure 9

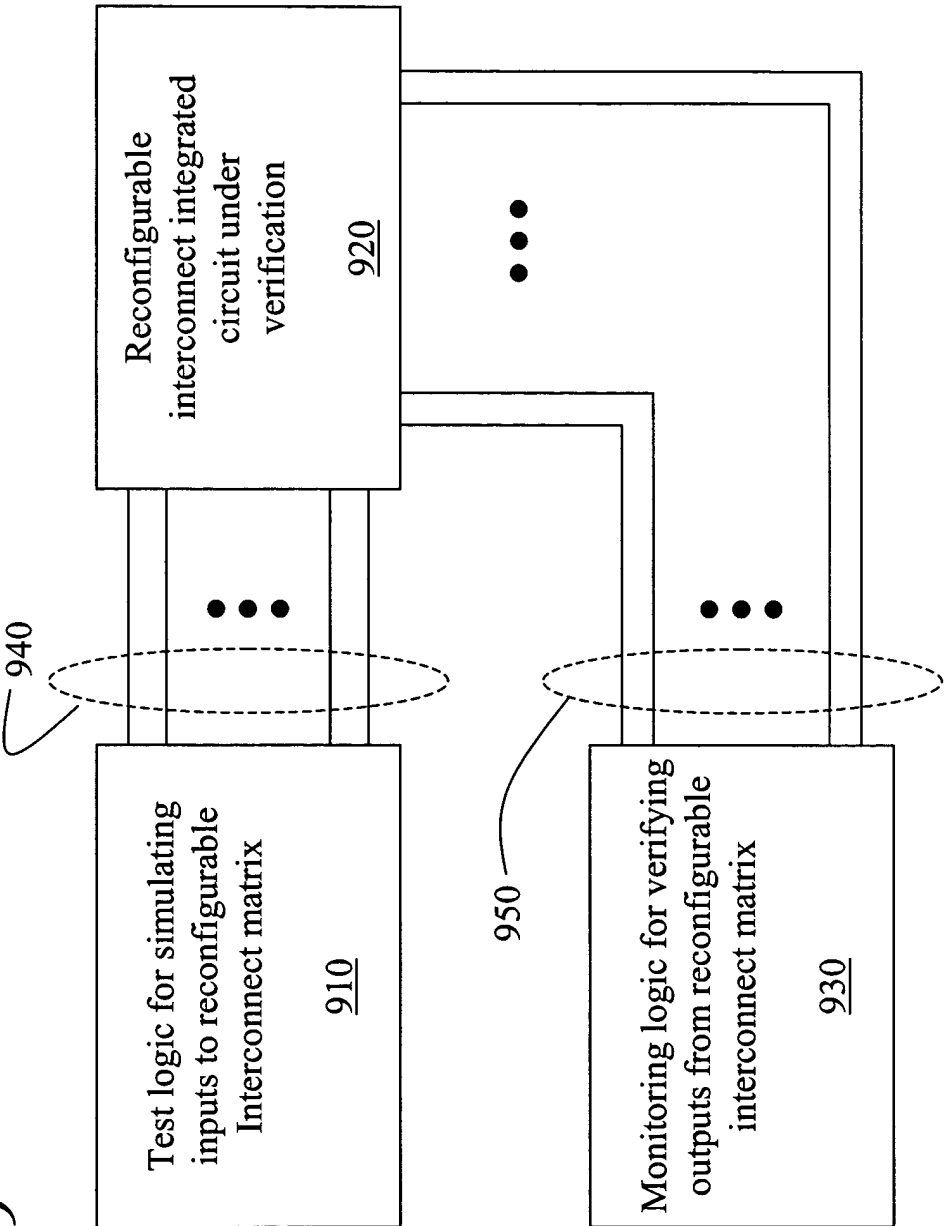


Figure 10

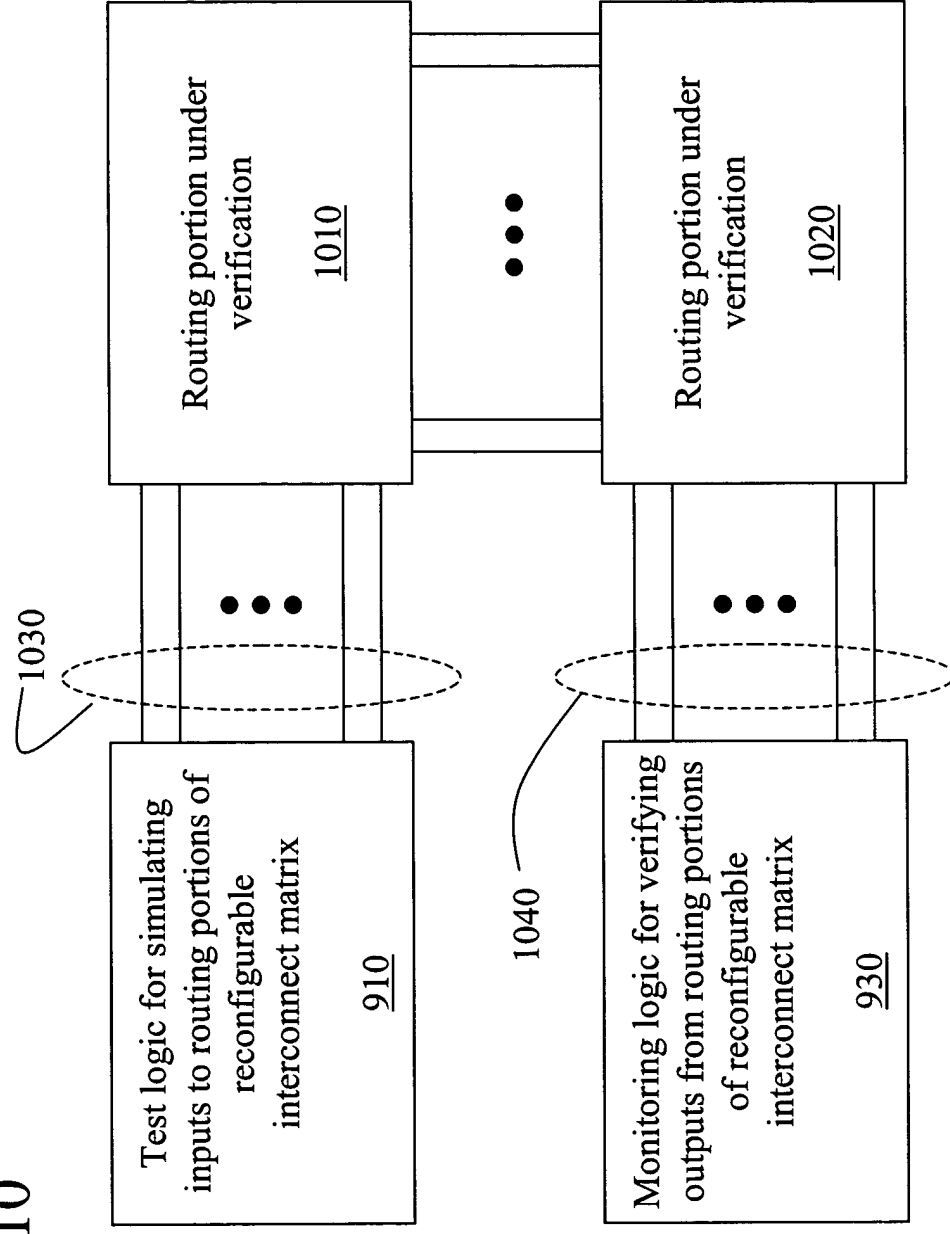
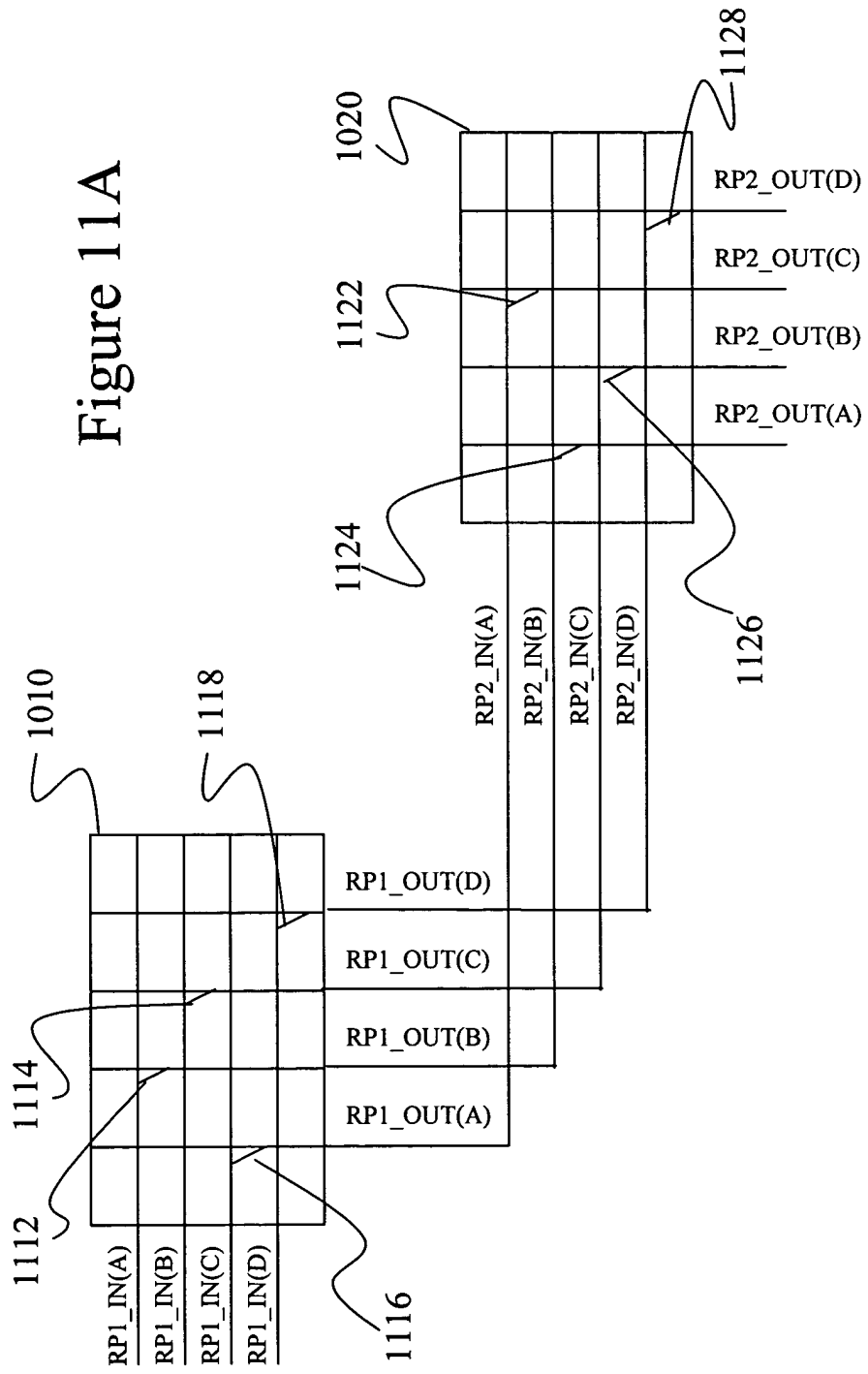


Figure 11A



# Figure 11B

|      | Input RP1 | Output RP1 |
|------|-----------|------------|
| 1112 | A         | B          |
| 1114 | B         | C          |
| 1116 | C         | A          |
| 1118 | D         | D          |

# Figure 11C

|      | Input RP2 | Output RP2 |
|------|-----------|------------|
| 1122 | A         | C          |
| 1124 | B         | A          |
| 1126 | C         | B          |
| 1128 | D         | D          |

Figure 12

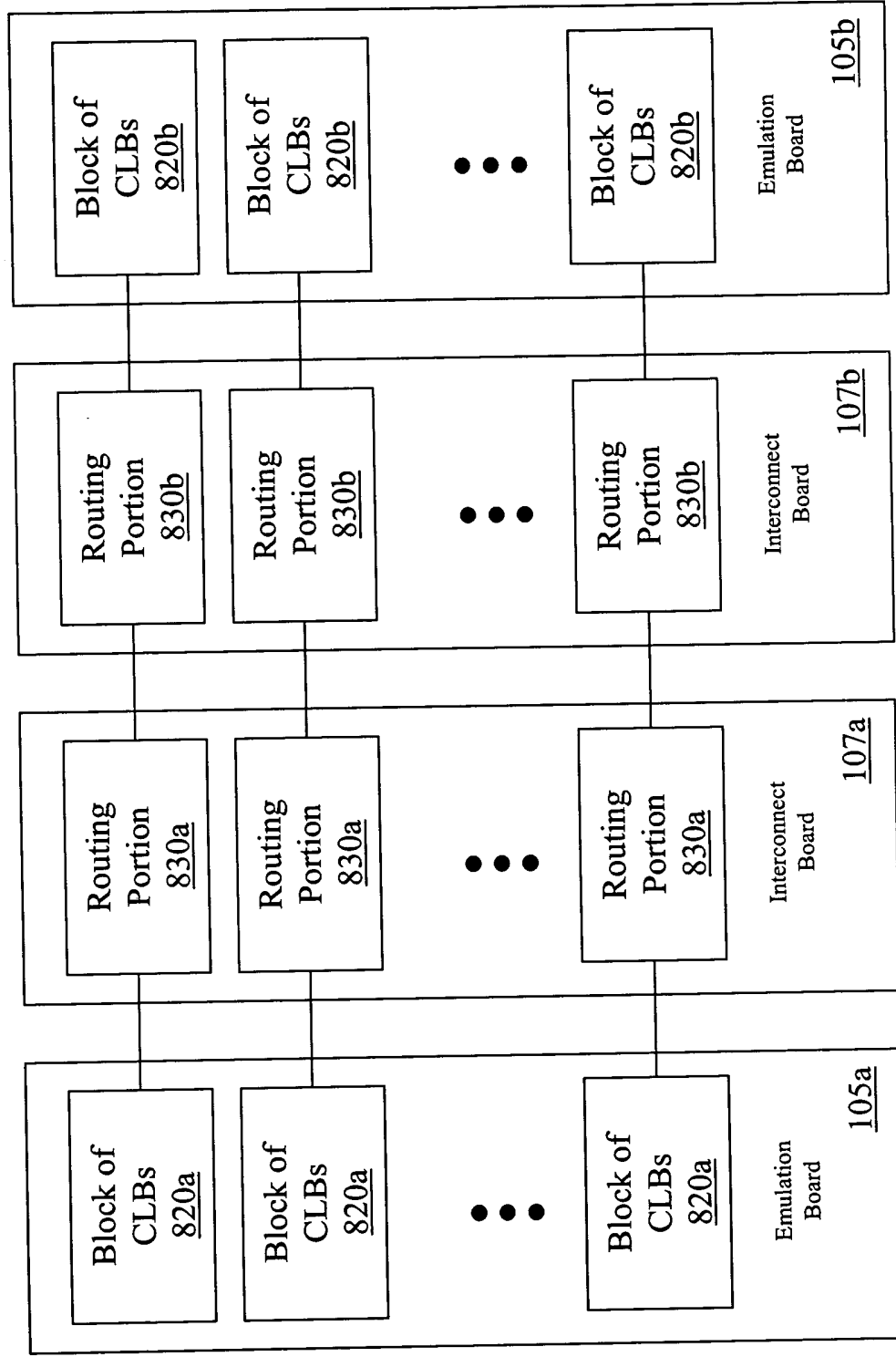


Figure 13A

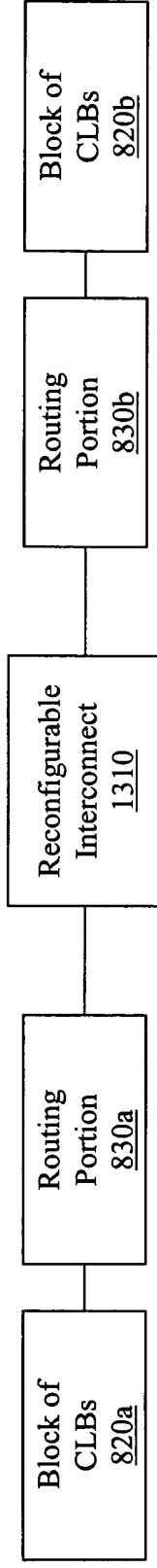


Figure 13B

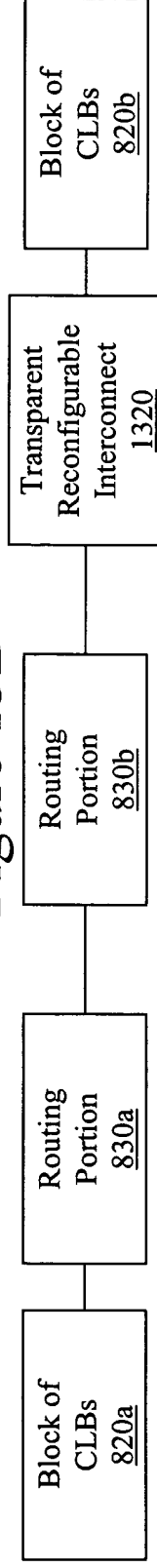


Figure 13C

